Variations of SNMs in Sub-threshold Circuits

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***Abstract*— Sub-threshold operation offers a compelling solution for ultra-low energy applications such as micro-sensors and embedded medical applications, where low energy needs are the primary concern instead of speed. By lowering the supply voltage below the transistors' threshold voltage, we see a dramatic drop in energy consumption when compared to normal operations, but circuit instability and delay variability are increased in sub-threshold operation. We must stabilize and mitigate the sensitivity to variation for optimal operation. This project explored variability metrics and noise sensitivity of cascaded logic gates. With the help of *HSPICE*, an analog circuit simulator, we were able to conduct DC analysis of circuits. We were then able to calculate the SNM, static noise margin, of two cascaded logic gates; this in-turn was used to study the robustness of a circuit at reduced supply voltages through Monte Carlo simulations.**

***Keywords*— Sub-threshold digital circuits; ultra-low energy; static noise margin; voltage scaling; variations;**

I. Introduction

Power efficiency and consumption recently have been becoming important factors in designing CMOS integrate circuits [1]. Power constraints have become an important factor for embedded applications due to the need for longer lifetimes. These applications such as micro-sensors and embedded medical devices require very-low energy because of their small form-factors and extended lifetimes.

Sub-threshold digital design offers a compelling solution for ultra-low energy applications because dynamic energy consumption is reduced exponentially with V_{dd}; the minimum energy operation point also usually occurs in the sub-threshold region [2] [3]. Although sub-threshold operation is a great option for power constrained applications, there are also downsides when operating in the sub-threshold region. CMOS circuits are more sensitive to noise and variations. Their on-off current ratios are also reduced. This paper analyses sub-threshold CMOS circuits' downsides.

The input voltage giving power to sub-threshold CMOS circuits is set below the transistor's threshold voltage V_t to obtain substantial amount of energy saved when speed is not the primary concern. Since sub-threshold CMOS circuits rely mainly on leakage currents, these circuits are more sensitive to variation because the leakage currents are exponentially dependent on V_t [4]. V_t variations are also increased when we use minimum size devices for sub-threshold operation; therefore, these CMOS circuits would not function properly due to insufficient output swings for a solid level logic. The need to upsize transistors begins to increase so that we can improve robustness and stability of CMOS circuits even at the expense of increased energy consumptions. Variability becomes an important factor when designing sub-threshold digital circuits.

The focus of my research was on the analysis of the downsides of sub-threshold circuits. In particular, my research looked at variation in SNMs. All DC analyses were done via HSPICE, a circuit simulation program. Python, a scripting programming language was the primary system to compute the analysis.

II. Logic Stability Metric

This section discusses about a metric called SNM (Static Noise Margin). SNM is used to determine the logic stability of CMOS logic gates. SNMs are useful because they tell us how much noise can a CMOS circuit handles before some logic gates start outputting logic failures. Therefore, SNM can be a consistent metric that can tell us if a logic gate has sufficient output swings (V_{OL}, V_{OH}).

Instead of using arbitrary limits such as 10% and 90% of V_{dd} as exampled in Fig. 1, we will be using butterfly plots to verify the actual output voltage levels.

2A. Butterfly Curve (Plots)

Butterfly curves can be generated by superimposing a logic gate's VTC (Voltage Transfer Characteristic) with the following logic gate's mirrored VTC. For simplicity, a 4-input NAND gate and a 4-input NOR gate was used to show the worst cases of output swings. The NOR gate has the most stringent VIL requirements and similarity the NAND gate has the most stringent VIH requirements [4]. Fig. 2(a) and Fig. 2(b) show the difference between sufficient outputs swings verses failing output swings. In Fig. 2(a), the NAND gate has sufficient output swing such that its V_{OL} produces a logic high output in the NOR gate. In contrast, in Fig. 2(b), the NAND gate exhibits a VOL of 160mV and produces a NOR output of 175mV, which is causing a logic failure.

We can now define logic failure as having no inscribed square in the butterfly curve. Since each side of the square is the same length, the measurement of one side of the square is the SNM. With these metrics, we can study the downsides of

sub-threshold circuits by analysing SNMs of different combinations of logic gates.

2B. Computation of SNM From Butterfly Curves

With the butterfly curves computed and stored as data points, we can use these two set of data points to compute the SNM. Since the sides of the SNM square has to be parallel to the x and y axis, we can deduce that the diagonal segment in the square has a slope of 1.

By iterating through a set of data points, I can compare the line segment created by the current data point with another data point from the mirrored second set of data points. If there is no line segment with a slope of 1, interpolation is used to determine a new data point between two real data points so that a new line segment is created with a perfect slope of 1.

By obtaining the longest possible line segment with a slope of 1, we have found a SNM square within the butterfly curve. The SNM can then be easily obtained through simple geometry and algebra using the two data points that represent the line segment

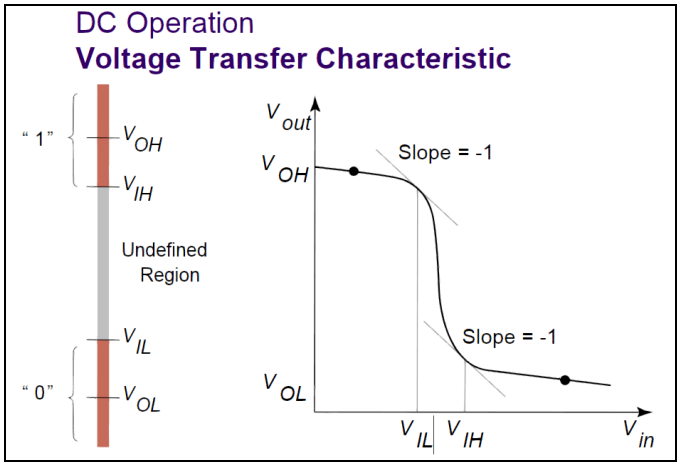

Fig. 1: VTC Example

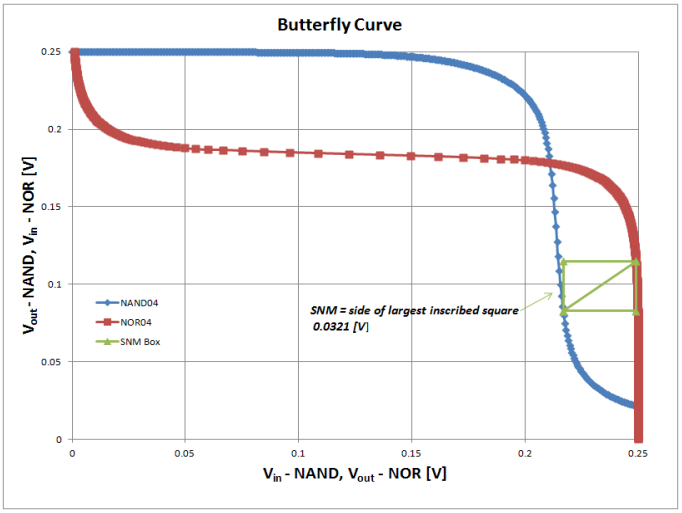

Fig. 2(a): Butterfly Curve of NAND04 and mirrored NOR04 (FUNCTIONING LOGIC)

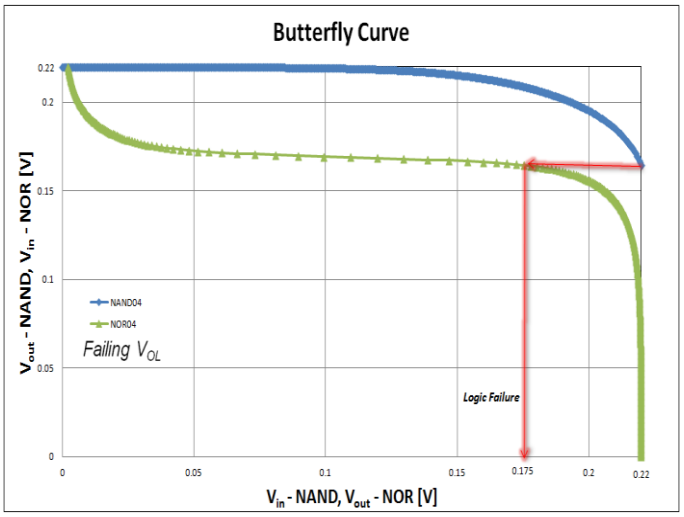

Fig. 2(b): Same Logic gates with slightly different V_{dd} (FAILING LOGIC)

III. SNM Variability

To observe the downsides of sub-threshold circuits, cases were examined to determine the problem depth when we are dealing with sub-threshold circuits. All simulations were done on different combinations of logic gates, but only the worst cases were shown in this report. The worst case logic gates used were 4-input NAND and NOR gates. The threshold voltages used for the transistors were about 400mV. We ran simulations on these circuits with a supply voltage of 1V to a supply voltage of 250mV.

3A. Variation in SNM Between Inputs of Logic Gates

The objective of this case is to investigate the variation in SNM between each input of a 4-input logic gate. By conducting DC analysis on each input of each 4-input logic gate, we were able to gather 8 different VTC curves, 4 per logic gate. By comparing the first logic gate's VTC curves against the second logic gate's mirrored VTC curves, we are able to generate 16 different combinations of butterfly curves. From the 16 butterfly curves, comes 16 different SNMs for this pair of 4-input logic gates. We converted the SNMs into percentages of its supply voltage and plotted the data into a line graph shown in Fig. 3.

Under normal operations with supply voltages being above the transistors' threshold voltage, the percentage difference of the worst case input to the input's average is below 0.5%; this is negligible. This is not the case as we lowered the supply voltage below the threshold voltage. As the supply voltage goes below V_t, the percentage difference start to increase at a steep pace. At 250mV, the percentage difference reaches over 3%; this is a potential problem for designers because each input of a logic gate will be at least 3% different from another input of the same logic gate.

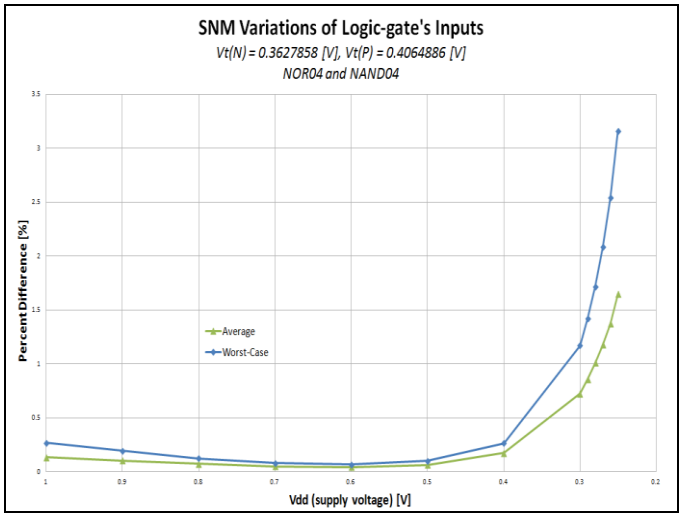

Fig. 3: SNM variation between inputs

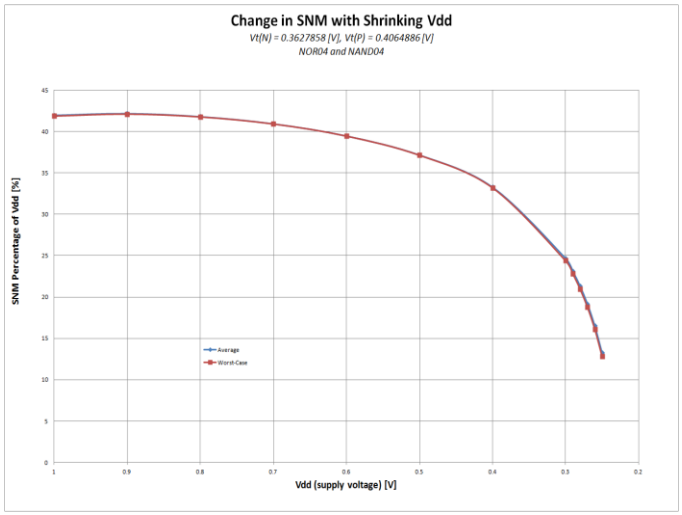

Fig. 4: Change in SNM as V_{dd} decreases

3B. Behavior in SNM as Vdd Decreases

The objective of this case is to investigate the behavior of sub-threshold circuits as the supply voltage is reduced below the threshold voltage. We wanted to confirm the behaviors of sub-threshold circuits through the analysis of SNMs when the supply voltage is shrinking.

We kept the transistor technology and logic gates the same throughout the simulation. The only variable that was changed was the supply voltage V_{dd}. We started with a supply voltage of 1V and started reducing it by 100mV until the logic begins failing. When we got to 300mV, we began lowering the voltage by 10mV; eventually we ended at 250mV being the lowest supply voltage before the circuit is non-functional.

The data is compiled and graphically represented as a line graph in Fig. 4. We represented the y-axis as SNM percentage of V_{dd} and the x-axis as the supply voltage. Under normal conditions well above the threshold voltage, the SNM percentage was above 40% of the supply voltage. This is a very good percentage because this would only leave the undetermined region to be 20% of the supply voltage. But as we lower the supply voltage below the threshold voltage, the SNM percentage began to drop exponentially. For a supply voltage of 300mV, the SNM percentage is already 25% of V_{dd}. For V_t = 250mV, the SNM percentage dropped to 12% of V_{dd}. The results were not surprising because we knew the stability of sub-threshold circuits is sketchy. SNM was a criterion for circuit stability. This result only proves that stability is greatly diminished as the supply voltage is reduced below the transistors' threshold voltage.

IV. Conclusion

In this paper, we investigated the some downsides to sub-threshold circuits such as variation. As we lower the supply voltage to a CMOS circuit, the stability decreases exponentially, especially when the supply voltage is reduced below the transistors' threshold voltage. We also discovered that there are variations between different inputs of a logic gate. This could be a potential issue for sub-threshold circuit designers because they would need to incorporate the variation of stability between the inputs of logic gates. There are other downsides to sub-threshold circuits, but we did not have time to investigate any further.

There are many future work; we need to investigate other downsides to sub-threshold circuits. We must also look into possible solutions to stabilize sub-threshold circuits so that they can be used in the industry. Increasing the size of transistors is a possible solution to improve stability of sub-threshold circuits but at the cost of higher power consumption. This is an acceptable loss if we can make sub-threshold circuits a compelling solution to the world's future needs.

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