Physical Design of Rachael SPARC

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Motivation & Goals

- UCSC's Very Large Scale Integration (VLSI) lab designs high-performance resonant clocks for synthesis on chips built from CMOS technology.
- The lab has access to 45nm technology and thus needs a microprocessor design at this scale so the tools in development can be tested in a real system.

History & Foundations

- The original microcontroller being modified is Rachael SPARC. This is an open source, 32-bit micro developed for commercial and academic use. It is written in verilog and developed for 180nm technology.
- Micro Architecture Lab Santa Cruz (MASC) picked up Rachael, changed its technology to 90nm and modified its memory.
- MASC has not worked with the place and route or floorplanning of the design.

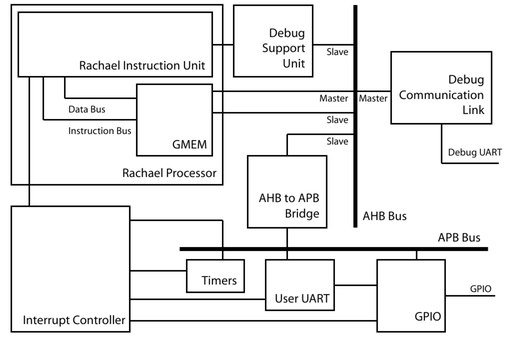


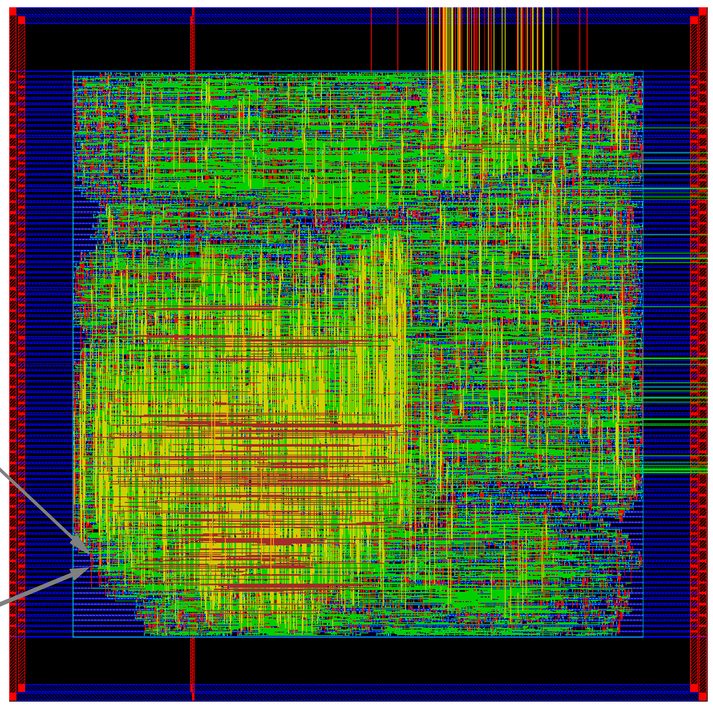
Fig. 1. Rachael SPARC Architecture block diagram

Initial Results

- Synopsys Design Compiler at 90nm:

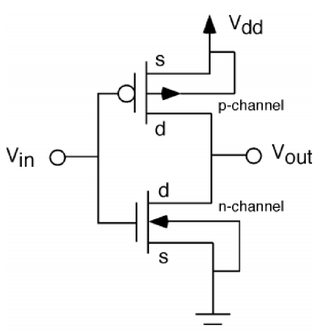
Critical Path Length:	0.88ns
Critical Path Slack:	-0.27ns
Critical Path Clk Period:	0.71ns
Cells:	14901
Hierarchical:	55
Leaf:	14846
Sequential:	3213
Combinational:	11632

- Cadence First Encounter at 90nm:
  Results from synthesis up until Clock Tree Synthesis. This is an incomplete layout of the components making up Fig. 1.

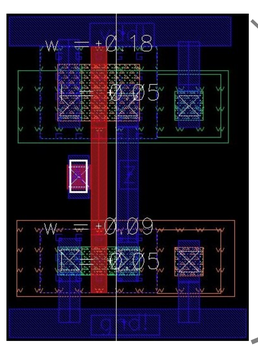


Explanation of Encounter Image

Schematic of an inverter

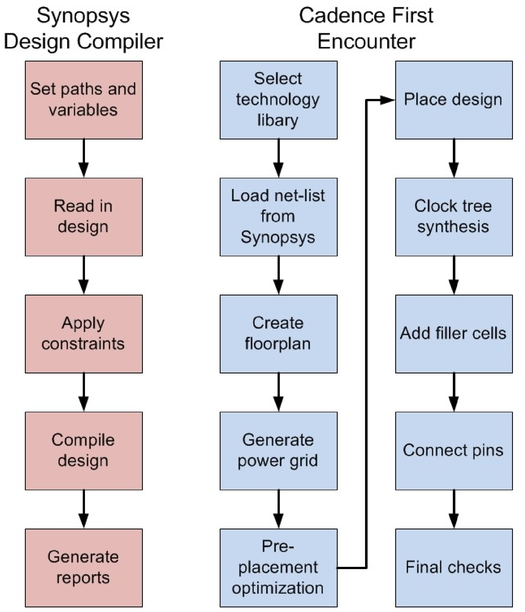


Layout of an inverter



http://cnx.org/content/m1029/latest/4.48.png
https://vlsiwiki.soe.ucsc.edu/images/5/53/20-add_taps.jpg

Tools



Future Work

- Complete design flow using Encounter
- Swap the 90nm libraries for 45nm
- Contribute to VLSI wiki

References

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- Fig. 1. Michael Cowell, Adam Postula, "Rachael SPARC: An Open Source 32-bit Microprocessor Core for SoCs," dsd, pp.415-422, 9th EUROMICRO Conference on Digital System Design (DSD'06), 2006