SRAM Memory Compiler

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Motivation

- Give system level designers access to multiple layers of abstraction for a given memory array.

- Allow for better characterization of memory before it is fabricated on the chip.

- Give designers access to an open source development tool.

How it Works

- Program takes in 3 parameters: Total size, word size, and memory name.

- The program determines layout necessary for the array as close to square as possible; in other words how many words per row.

- The program then tiles the bit cells out to form the rows and columns of the array

- The compiler then tiles out the peripheral hardware for the memory to function.

- Lastly, just like the above, the compiler constructs a spice net-list for front end simulation with estimated parasitics.

Current Work

LVS Checking

Once design is LVS clean, the design can be run through back annotation and the parasitics can be extracted from the design. This allows the user to run back end simulation to better characterize memory.

Automated Timing Specs

Once the array has been constructed, this tool would then be able to find proper timing parameters for running the memory.

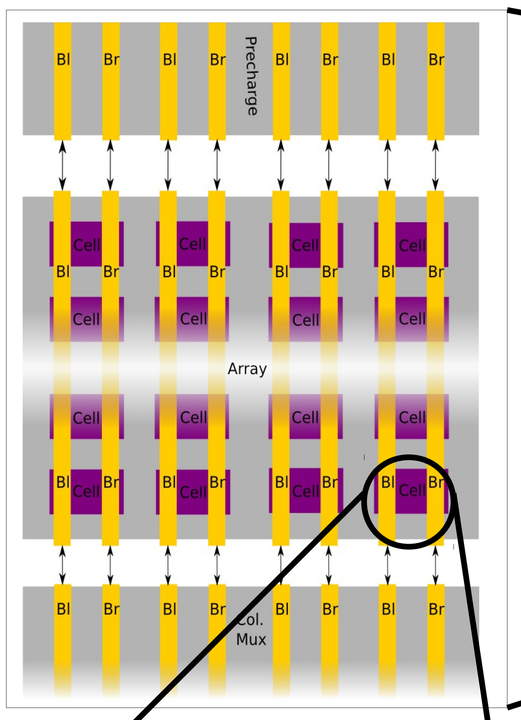
Variability

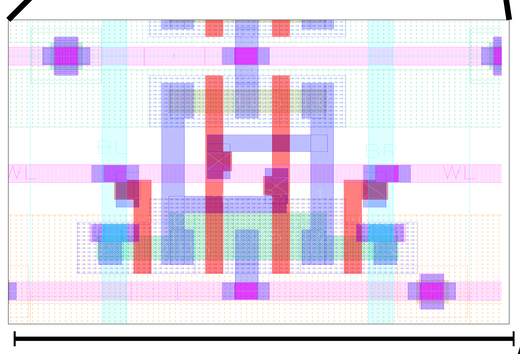
Predict how the memory will behave after process variation has been accounted for and how the memory will behave under environmental noise.

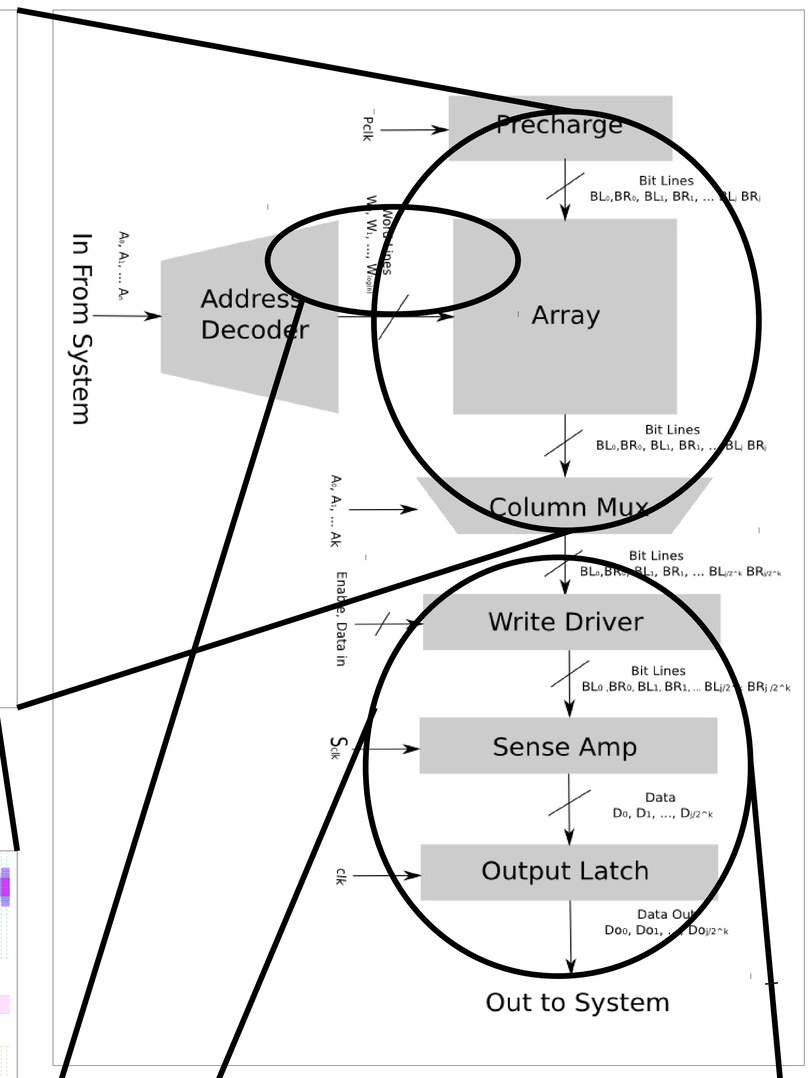
Future Work

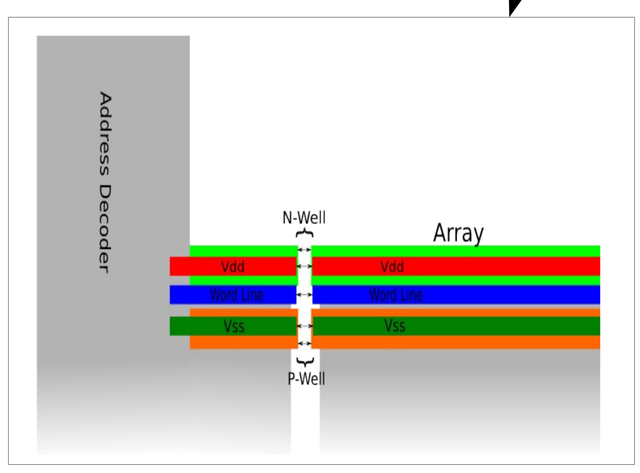
- Reliability through redundant columns and rows

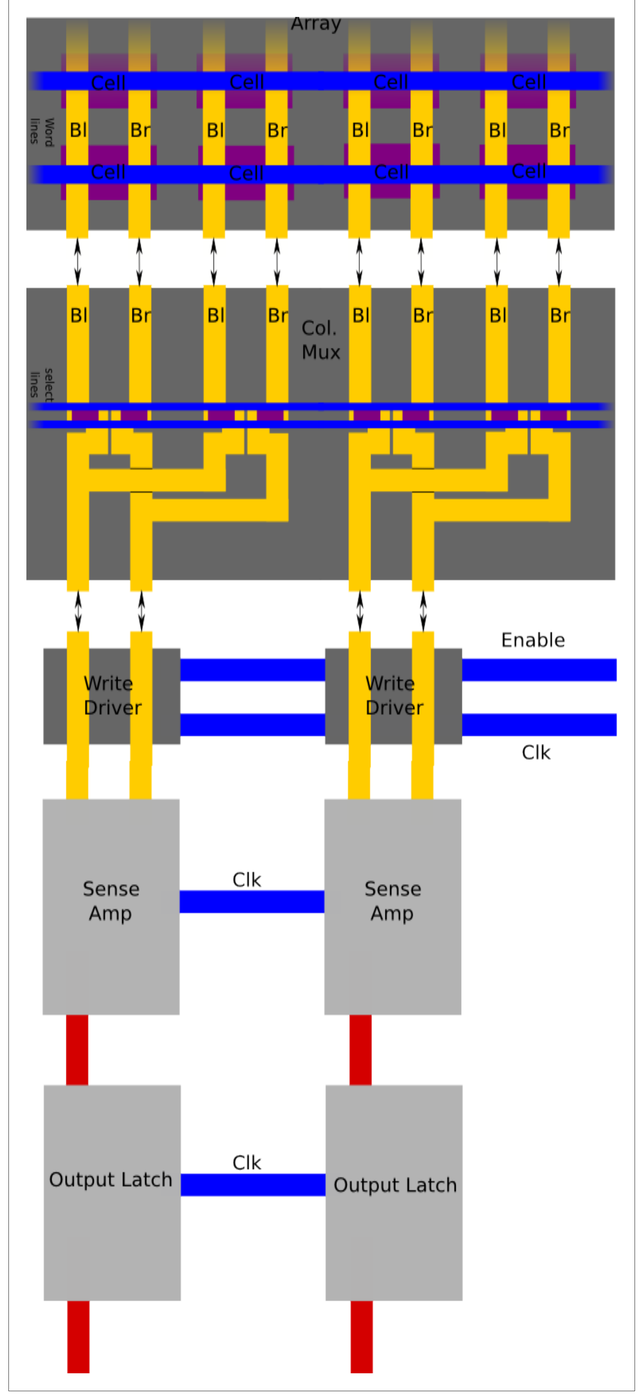
- Support of many different memories besides the standard 6 transistor SRAM.











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