FPGA OVERCLOCKING
Developing a Platform to Model IC Variability

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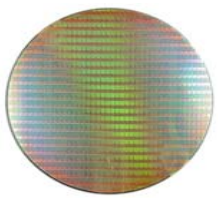
OVERVIEW

The goal of this project is to implement a platform that will be used to model and validate of the effects of process variation which may occur during manufacturing. In modern chip fabrication processes (65nm and smaller) variability not only introduces timing inconsistency across dies, but also timing uncertainties inside a single die. Therefore variability-induced issues in modern IC designs are becoming a first-class design concern and comprise a complex set of correlated statistical distributions. In order to better deal with the effects of variability, via improved design for manufacturing techniques, improved process refinements, and better architectural approaches, designers need better models and understanding of the sources and effects of variability.

Most approaches to model variability among the academic community have been mainly theoretical in nature, with little or no empirical validation. The main reason for this is the prohibitive costs associated with modern CMOS fabrication technologies, with modern *fab lines costing several billion dollars each.

To avoid the financial penalty of having to fabricate custom IC layouts to test and model variability, we propose the utilization of Field Programmable Gate Arrays (FPGAs) to be used as a first order approximation vehicle for the development and evaluation of variability distribution maps.

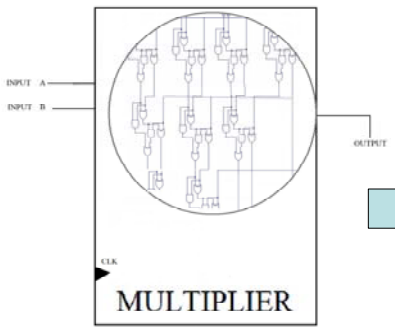


Silicon wafer

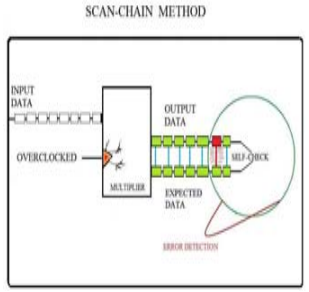
APPROACH

Our approach evaluates the failure points across the area of the FPGA. To do this, we replicate a common circuit, in this case a multiplier, through the fabric of logic. Each multiplier is implemented in a specific (bounded) section of the FPGA and receives a common clock signal for the whole chip. In order to evaluate failure points, we overclock the FPGA and evaluate which circuits fail to meet the timing constraints. A mapping function relays the information regarding which circuit failed, and where in the FPGA circuit is located. This allows the experiment to generate a simple failure distribution which allows for an intuitive mapping of frequency to the distribution of faults across the chip's area.

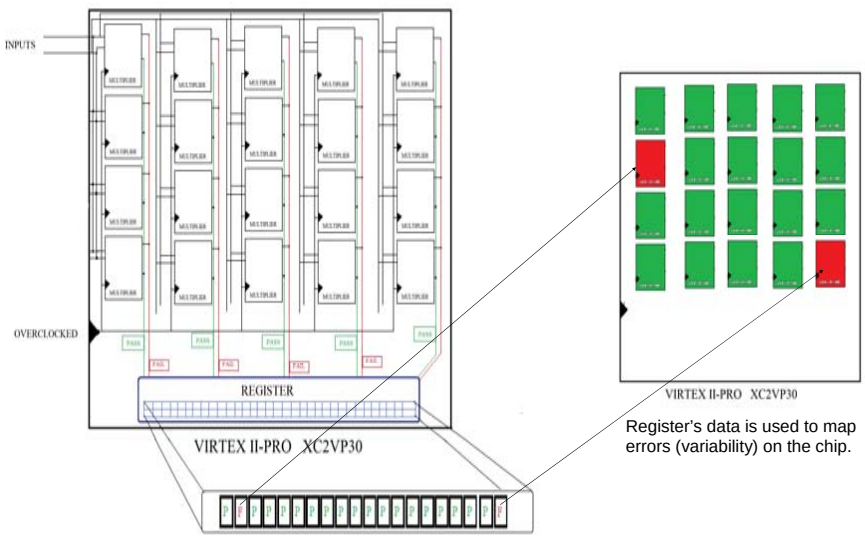
PROTOTYPE



6-bit multiplier reads the input data from a ROM file.



Scan-chain method is used in each multiplier to automatically detect errors. Errors are expected at extreme high frequencies (overclocked).

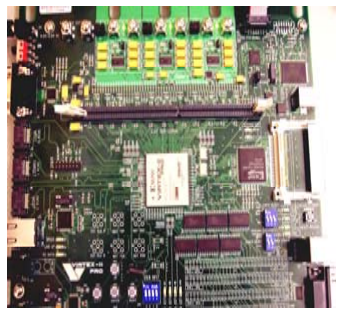


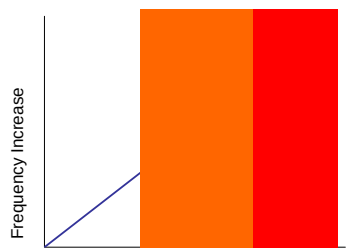
Register's data is used to map errors (variability) on the chip.

The diagram illustrates 25 multipliers in the chip, which occupies 819 **slices out of 13,696 available. Each multiplier is formed by 32 slices. After the chip is overclocked, a set of results is sent to the register where all results are stored.

MATERIALS

- FPGA VIRTEX II- PRO
- Xilinx ISE 9.2
- ModelSim - verilog simulator
- Clock Generator
- Frequency Analyzer





Frequency diagram represents the expected behavior of the number of multipliers failing as the frequency increases.

**slice: a programmable unit which contains latches and flip-flops

REFERENCES:
Silicon Wafer: image:http://www.hardwarezone.com/img/data/articles/2004/1106/pentiumm_wafer.jpg