Standing Wave Oscillators for Global Clock Distribution

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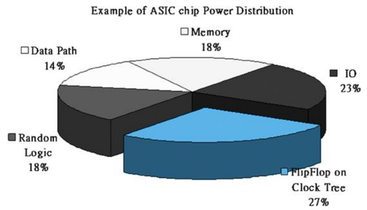
1 Motivation and Goal

- Clocks are power-hungry, consuming up to 40% overall processor power
- Energy reflected off of loads is currently ignored
- High-frequency designs will require transmission line analysis
- **Goal**: implement a standing-wave oscillator (SWO) sizing algorithm into UCSC VLSI-DA's Clocksyn project
  - Combine with other power-saving methods

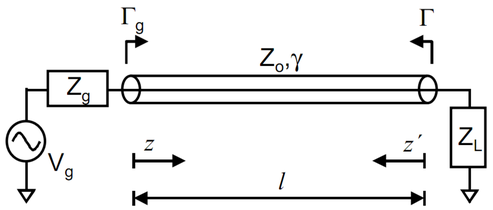


Power consumption in a typical ASIC

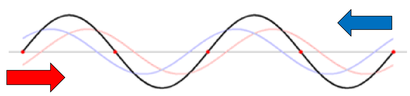
Image: http://www.synopsys.com.cn/information/snug/2010/using-multi-bit-flip-flop-for-clock-power-saving-by-designcompiler

2 Theory

- Electrical signals travel gradually across a wire, not instantaneously
- Said signals (incident waves) bounce off of impedance mismatches back to their source and can form standing waves



Voltage source with series impedance, transmission line, sink impedance; reflections happen when impedances are not equal



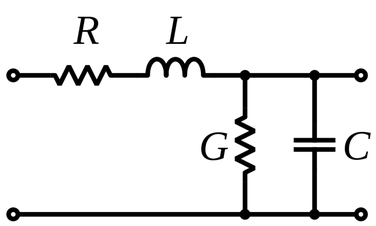
Incident wave (red) and reflected wave (blue) creating a standing wave (black)

- Standing waves use the reflected wave to conserve energy
- Previous work: board-level implementation [1], chip-level [2]
- More work to be done with nonuniform trees

1. V.L. Chi, "Salphasic distribution of clock signals for synchronous systems," IEEE Trans. Comput., vol. 43, pp.597−602, May 1994.
2. Frank O'Mahony, "Design of a 10GHz Clock Distribution Network Using Coupled Standing-Wave Oscillators," Proceedings of DAC 2003, pp. 682-687, 2003.
Images: [2], http://en.wikipedia.org/wiki/Standing_wave

3 Methods

- Model wires as distributed uniform, lossy transmission lines



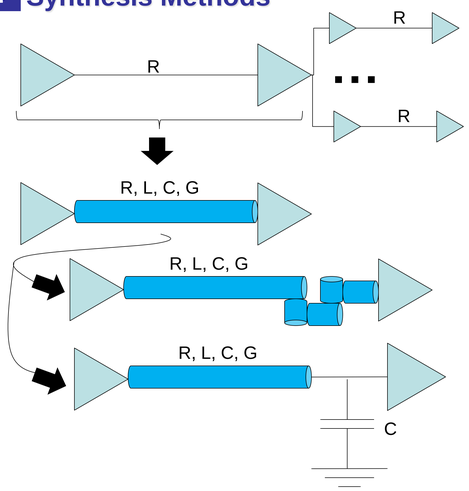
$$\gamma = \sqrt{(R + j\omega L)(G + j\omega C)}$$
$$\mathrm{Re}(\gamma) \approx \frac{\sqrt{LC}}{2}\left(\frac{R}{L} + \frac{G}{C}\right)$$
$$\mathrm{Im}(\gamma) \approx \omega\sqrt{LC}$$

Transmission lines are modeled as an infinite series connection of this schematic; formulas at right are used in measuring the signal attenuation and phase shift due to the transmission line

- Use propagation constant γ and approximations to measure attenuation and phase shift
- Model sink as open circuit and eventually branch impedance
- Send 10GHz sine wave across circuit and observe sink voltage
- Simulator: NGSpice 23, HSpice
  - LTRA / W: Distributed uniform lossy transmission line

Images: http://en.wikipedia.org/wiki/Transmission_line

4 Synthesis Methods

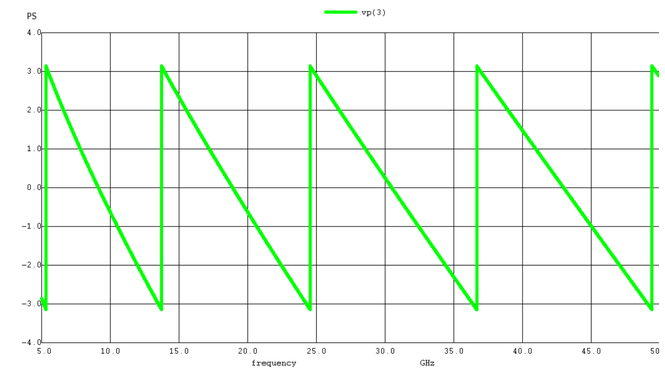


- Replace existing global wires with transmission line models
- Calculate transmission line phase shift using the phase constant β
- Resize (snake) transmission line if necessary

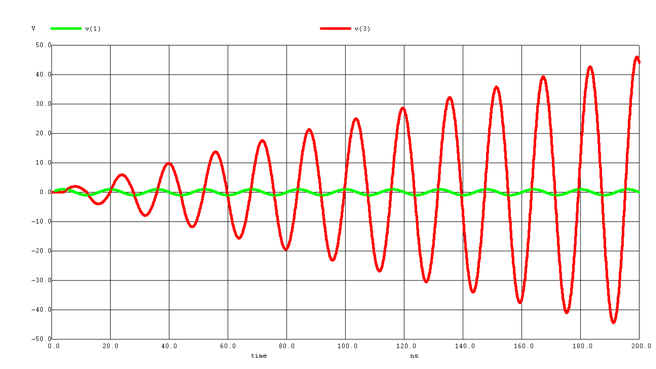
and/or

- Add capacitors before sinks as needed for additional phase shift
- Calculate reflection coefficient based off of branch impedance and transmission line impedance
- Investigate cross-coupled inverters to offset voltage degeneration

5 Results and Challenges



Phase shift vs. frequency for a given wire; resonant frequencies are marked by their pi-radian phase shift



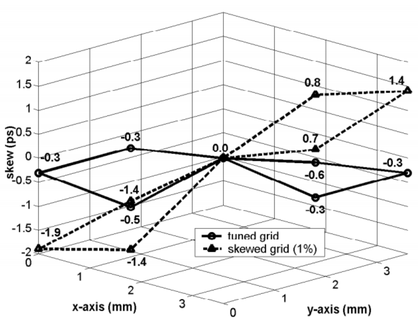
Properly matched phase shift; signal reflection forms a standing wave that keeps growing

- Resonant frequency calculated and identified
- Ringing too strong with open-circuit termination; realistic admittance G will dampen
- NGSpice transmission line yields erroneous results for RLGC line[1]; HSpice necessary

[1] http://ngspice.sourceforge.net/docs/ngspice23-manual.pdf, pg. 91

6 Ongoing Work

- Develop algorithm to adjust wirelength for better phase shift
- Investigate using a capacitance to phase shift as needed
- Match impedances to maximize power transfer
- Investigate cross-coupled inverters to cancel attenuation
- Implement findings into Clocksyn source code



Desirable low SWO skew, mostly in the sub-picosecond range - no more than 1.9% of the clock period, compared to the 10% target of modern designs.

Image: Frank O'Mahony, 10GHz Global Clock Distribution Using Coupled Standing-Wave Oscillators, August 2003.

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